Drawing No.: RLP-K-HTS-0002 /1

Date: 2025. 1. 7

Data sheet

Title: METAL-PLATE CHIP RESISTOR; LOW OHM

Style: RLP16,20,32,63

AEC-Q200 qualified

RoHS COMPLIANCE ITEM Halogen and Antimony Free

Note: •Stock conditions

Temperature: $+5^{\circ}\text{C} \sim +35^{\circ}\text{C}$ Relative humidity: $25\% \sim 75\%$

The period of guarantee: Within 2 year from shipment by the company.

Solderability shall be satisfied.

- Product specification contained in this data sheet are subject to change at any time without notice
- •If you have any questions or a Purchasing Specification for any quality agreement is necessary, please contact our sales staff.



Hokkaido Research Center Approval by: T. Sannomiya Drawing by: M. Shibuya

Title: METAL-PLATE CHIP RESISTOR; LOW OHM

RLP16, 20, 32, 63 Page: 1/12

Style

1. Scope

1.1 This data sheet covers the detail requirements for metal-plate chip resistor; low ohm, style of RLP16, 20, 32, 63.

1.2 Applicable documents

JIS C 5201-1: 2011, IEC60115-1: 2008, AEC-Q200 Rev.D

2. Classification

Type designation shall be the following form.

(Example)

RLP	63	K	R010	F	TE
1	2	3	4	5	6
Sty					

1 Metal - plate chip resistor; low ohm

2 Size

RLP16	1608 size
RLP20	2012 size
RLP32	3216 size
RLP63	6332 size

3 Temperature coefficient of resistance

N	±70×10 ⁻⁶ / °C
K	±100×10 ⁻⁶ / °C
–(Dash)	Standard

4 Rated resistance

1L50	1.5mΩ
R002	2mΩ

5 Tolerance on rated resistance

F	±1%
J	±5%

6 Packaging form

TP	Paper taping
TE	Embossed taping



METAL-PLATE CHIP RESISTOR; LOW OHM

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3. Rating

3.1 The ratings shall be in accordance with Table-1.

Table-1(1)

			Table-1(
Style	Rated dissipation (W)	Rated current (A)	Temperature resistance	coefficient of (10 ⁻⁶ / °C)	Rated resistance (mΩ)	Tolerance on rated resistance		
5.5.4		8.1	K N	±100 ±70	5			
RLP16	0.33	5.7	K N	±100 ±70	10			
		15.8	K N	100	2			
		11.1	K	±70 ±100	4			
			N K	±70 100				
		10.0	N K	±70 ±100	5			
RLP20	0.5	9.1	N	±70	- 6			
		7.9	K N	100 ±70	- 8			
		7.4	K N	±100 ±70	9			
		7.0	K N	±100 ±70	10			
		31.6	Standard K	±150 ±100	1			
		22.3	K N	±100 ±70	2			
		18.2	K N	±100 ±70	3	F(±1%)		
		15.8	K N	±100 ±70	4	J(±5%)		
		14.1	K N	±100 ±70	5			
				12.9	K N	±100	6	
		11.9	K	±70 ±100	7			
RLP32	1.0	11.1	N K	±70 ±100	8			
		10.5	N K	±70 ±100	9			
		10	N K	±70 ±100	10			
		9.5	N K	±70 ±100	11			
			N K	±70 ±100	12			
				9.1	N K	±70 ±100		
		8.7	N K	±70 ±100	13			
		8.4	N K	±70	14			
		8.1	N N	±100 ±70	15			

Title: METAL-PLATE CHIP RESISTOR; LOW OHM

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Table-1(2)

Style	Rated dissipation (W)	Rated current (A)	Temperature resistance	coefficient of	Rated resistance (mΩ)	Tolerance on rated resistance
	2.0		Standard	±150		
		44.7	K	±100	1	
			N	±70		
		22.3	K	±100	2	
		22.3	Ν	±70	2	
		18.2	K	±100	3	
		10.2	N	±70	3	F(±1%) J(±5%)
		15.8	K	±100	4	
		10.0	N	±70	7	
	1.0	14.1	K	±100	5	
			N	±70	, and the second	
		12.9 11.9	K	±100	6	
RLP63			N	±70	•	
			K	±100	7	
			N	±70		
		11.1	K	±100	8	
		10.5	N	±70	-	
			K	±100	9	
			N	±70	-	
		10	K	±100	10	
			N	±70		
		9.1	K	±100	12	
			N	±70		
		8.1	K	±100	15	
		0.1	N	±70	_	

Style	Insulation voltage (V)	Category temperature range (°C)
RLP16		
RLP20	100	−55~+155
RLP32	100	-55~+155
RLP63		

3.2 Derating

The derated values of dissipation at temperature in excess of 70 °C shall be as indicated by the following curve.

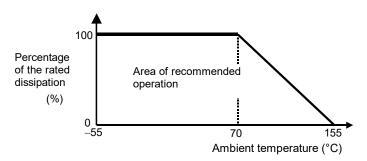


Figure-1 Derating curve



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3.3 Rated voltage

d.c. or a.c. r.m.s. voltage calculated from the square root of the product of the rated resistance and the rated dissipation.

$$E = \sqrt{P \cdot R}$$

E: Rated voltage (V)

P: Rated dissipation (W)

R: Rated resistance (Ω)

3.4 Rated current

The rated current calculated from the square root of the quotient of the rated resistance and the rated dissipation.

I: Rated current (A)

P: Rated dissipation (W)

R: Rated resistance (Ω)

The rated current shall be corresponding to rated voltage.

4. Packaging form

The standard packaging form shall be in accordance with Table-2.

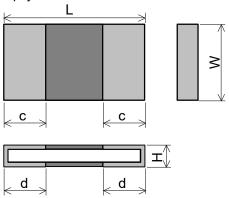
Table-2

Symbol	Packaging form		Standard packaging quantity / units	Application
TP	Paper taping	8mm width, 4mm pitches	5,000 pcs.	RLP16, 20, 32
TE	Embossed taping	12mm width, 4mm pitches	4,000 pcs.	RLP63

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5. Dimensions

5.1 The resistor shall be of the design and physical dimensions in accordance with Figure-2 and Table-3.

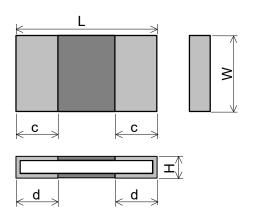


Figure_2

Table–3(1) Unit: mm

						Unit: mm
Style	Rated resistance (m Ω)	L	W	Н	С	d
RLP16	5	1.6±0.1	0.8±0.1	0.35±0.10	0.2±0.1	0.6±0.1
KLP10	10	1.0±0.1	U.O±U. I	0.3±0.1	0.2±0.1	0.3±0.1
	2			0.22±0.10	0.35±0.10	0.55±0.20
	4			0.35±0.10	0.35±0.10	0.75±0.20
	5			0.35±0.10	0.35±0.10	0.6±0.2
RLP20	6	2.0±0.15	1.25±0.15	0.35±0.10	0.35±0.10	0.47±0.20
	8			0.22±0.10	0.35±0.10	0.6±0.2
	9			0.22±0.10	0.35±0.10	0.52±0.20
	10			0.22±0.10	0.35±0.10	0.47±0.20
	1			0.32±0.15	1.1±0.25	1.1±0.25
	2			0.32±0.15	0.5±0.25	0.5±0.25
	3			0.35±0.10	0.7±0.25	1.3±0.25
	4			0.35±0.10	1.1±0.25	1.1±0.25
	5			0.35±0.10	1.0±0.25	1.0±0.25
	6			0.35±0.10	0.85±0.25	0.85±0.25
	7			0.35±0.10	0.7±0.25	0.7±0.25
RLP32	8	3.2±0.15	1.6±0.15	0.35±0.10	0.6±0.25	0.6±0.25
I NEI OZ	9	0.210.10	1.020.10	0.3±0.1	0.75±0.25	0.75±0.25
	10			0.28±0.10	0.5±0.25	0.5±0.25
	11]		0.28±0.10	0.5±0.25	0.5±0.25
	12			0.22±0.10	0.65±0.25	0.65±0.25
	13			0.22±0.10	0.65±0.25	0.65±0.25
	14			0.22±0.10	0.55±0.25	0.55±0.25
	15			0.22±0.10	0.5±0.25	0.5±0.25

RLP16, 20, 32, 63 Page: 6/12



Table–3(2) Unit: mm

Style	Rated resistance (mΩ)	L	W	Н	С	d
	1		3.2±0.25	0.38±0.15	2.2±0.25	2.2±0.25
	2		3±0.25 3.1±0.25	0.38±0.15	1.1±0.25	1.1±0.25
	3			0.45±0.15	2.2±0.25	2.2±0.25
	4			0.35±0.15	2.2±0.25	2.2±0.25
	5	6.3±0.25		0.34±0.15	1.95±0.25	1.95±0.25
DI Dea	6			0.34±0.15	1.75±0.25	1.75±0.25
RLP63	7			0.35±0.15	1.4±0.25	1.4±0.25
	8			0.35±0.15	1.1±0.25	1.1±0.25
	9			0.35±0.15	0.8±0.25	0.8±0.25
	10			0.23±0.15	1.75±0.25	1.75±0.25
	12			0.23±0.15	1.4±0.25	1.4±0.25
	15			0.23±0.15	0.95±0.25	0.95±0.25

5.2 Net weight (Reference)

5 \					
Style	Rated resistance (m Ω)	Net weight (mg)			
RLP16	5,10	2			
RLP20	2, 4 to 6 , 8 to 10	3			
RLP32	1 to 3	12			
KLF32	4 to 15	11			
DLDGO	1,2	47			
RLP63	3 to 10,12 15	43			

6. Marking

The Rated resistance of RLP16 should not be marked standard.

6.1 RLP63

The rated resistance shall be marked in 4 characters consisting of 3 figures and a letter and marked on over coat side.

(Example) "R010"
$$\rightarrow$$
 0.01 [Ω] \rightarrow 10 [m Ω]

"1L50"
$$\to$$
 0.0015 [Ω] \to 1.5 [m Ω]

6.2 RLP20, 32

The rated resistance shall be marked in combination of two figures and underlines and marked on over coat side.

(Example) "
$$\underline{05}$$
" \rightarrow 0.005 [Ω] \rightarrow 5 [m Ω]

"
$$\underline{10}$$
" \rightarrow 0.01 [Ω] \rightarrow 10 [m Ω]



Drawing No: RLP-K-HTS-0002 METAL-PLATE CHIP RESISTOR; LOW OHM

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7. Performance

7.1 The standard condition for tests shall be in accordance with Sub-clause 4.2, JIS C 5201–1: 2011.

7.2 The performance shall be satisfied in Table-4.

Table-4(1)

	T ("	1able-4(1)	Б.
No.	Test items	Condition of test	Performance requirements
1	High temperature exposure	MIL-STD-202 Method 108	Δ R/R: Within ±3%
	AEC Q200 - No.3	Ambient temperature:155±2°C,	No visible damage
		Condition: Without load,	
		Duration: 1,000 +48 h	
		Interval measurements: 250 h and 500 h	
2	Temperature cycling	JESD22 Method JA-104	Δ R/R: Within ±3%
	AEC Q200 - No.4 Temperature: -55±3°C / 155±2°C,		No visible damage
		Dwell time: 30min maximum at each temp.	
		Transition time: 1 min. max.	
		Number of cycles: 1,000 cycles.	
_	Dia a la maidit :	Interval measurements: 250 cy and 500 cy	- D/D 14/4 :
3	Bias humidity	MIL-STD-202 Method 103	Δ R/R: Within ±3%
	AEC Q200 – No.7	Condition: 85°C & 85% R.H.	No visible damage
		Test power: 10% of rated power shall be applied	
		for continuously.	
		Duration: 1,000 +48 h	
		Interval measurements: 250 h and 500 h	
4	Operational life	MIL-STD-202 Method 108	Δ R/R: Within ±3%
	AEC Q200 - No.8	Ambient temperature: 125±2°C	No visible damage
		The applied voltage shall be the voltage to be	
		calculated at 35% of rated dissipation or the	
		limiting element voltage whichever is the smaller.	
		Condition: The voltage shall be applied for	
		continuously.	
		Duration: 1,000 +48 h	
		Interval measurements: 250 h and 500 h	
5	External Visual	MIL-STD-883 Method 2009	Inspect device construction, marking
	AEC Q200 - No.9		and workmanship.
6	Dimensions	JESD22 Method JB-100	As in Table–3
	AEC Q200 – No.10		
7	Resistance to Solvents	MIL-STD-202 Method 215	Δ R/R: Within $\pm 1\%$
	AEC Q200 – No.12	Solvent: 2-propanol at 25°C	No visible damage
		Immersion time: 3 min	
		Brush: 10 times brushing	
		Immersion and brush cycle: 3cycle	
8	Mechanical Shock	MIL-STD-202 Method 213	Δ R/R: Within ±1%
	AEC Q200 – No.13	Waveform: half sine,	No visible damage
		Peak value100G,	
		Normal duration 6ms	
		Condition: XX'YY'ZZ', 18times total	



METAL-PLATE CHIP RESISTOR; LOW OHM

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Table-4(2)

No.	Test items	Condition of test	Performance requirements
9	Vibration	MIL-STD-202 Method 204	ΔR/R: Within ±1%
	AEC Q200 – No.14	Peak acceleration and Sweep time: 5 g's for 20 min,	No visible damage
		Frequency 10Hz to 2000Hz,	_
		Condition: 12 cycles each of 3 orientations	
10	Resistance to soldering	MIL-STD-202 Method 210	Δ R/R: Within ±3%
	heat	Test conditions:K	No visible damage
	AEC Q200 - No.15	Peak temperature: 250±5 °C, 30sec	
		Soldering time above 183 °C: 90 - 120sec	
		Temperature ramp: 1°C/s-4°C/s	
		Test times:3 times	
11	ESD test	AEC-Q200-002	Δ R/R: Within ±5%
	AEC Q200 – No.17	Human body model, 2 Kohm, 150 pF,	No visible damage
		Test voltage: 12kV	
12	Solderability	J-STD-002	The surface of terminal immersed
	AEC Q200 – No.18	B) Bake the sample for 155 °C dwell time 4h /	shall be min. of 95% covered with a
		solder dipping 235°C/ 5s.	new coating of solder.
		Solder: Sn96.5-Ag3-Cu0.5	
		B1) Bake the sample for 155 °C dwell time 4h /	
		solder dipping 245°C/ 5s.	
		Solder: Sn96.5-Ag3-Cu0.5	
		D) Category 3,	
		Solder dipping 260°C/ 30s.	

METAL-PLATE CHIP RESISTOR; LOW OHM

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Table-4(3)

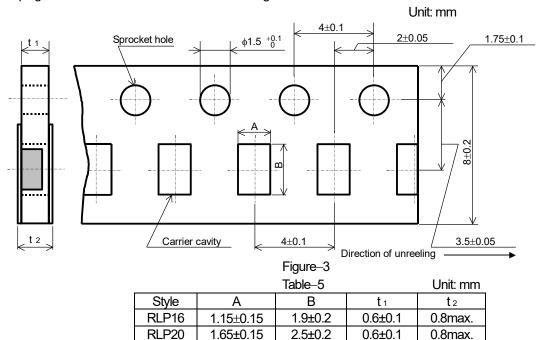
No	Test items	1	Condition (` '			Dorformanaa raguiramenta
No.		Condition of test				Performance requirements	
13	Electrical Characterization	1. D.C. Resistance				1. The resistance value shall	
	AEC Q200 - No.19		JIS C 5201-1 4.			4 4	correspond with the rated
		Mount it on our recommended 4-terminal test				resistance taking into account the	
		board and measure the resistance using the				specified tolerance.	
		4-terminal measurement method.				2. As in Table–1	
		Current Current Current Solder resist					
					l	Jnit:mm	
		Style	Resistance value(m Ω)	а	b	С	
		DI DIO	5	0.6	0.8	0.0	
		RLP16	10	1.0	0.6	0.9	
		RLP20	2 to 10	0.8	0.95	1.36	
			1	1.0	1.45		
			2	2.1	0.9		
		DI DOG	3	0.8	1.55	1.7	
		RLP32	4	1.0	1.45	1.7	
			5, 6	1.4	1.25		
			7 to 15	2.1	0.9		
			1	1.5	3.0	4.0	
			2	4.0	1.8		
		RLP63	3, 4	1.8	2.9	3.5	
			5	2.4	2.6	3.5	
			6 to 10,12,15	4.0	1.8		
		2. Temperature Coefficient of Resistance					
		-55 °C / +20°C					
		+20 °C / +	155°C				
14	Flammability AEC Q200 – No.20	UL-94					V-1 is acceptable
15	Bending strength	AEC-Q200-005				Δ R/R: Within ±1%	
	AEC Q200 – No.21	Bending value: 2mm			No visible damage		
		Holding tim					
16	Adhesion	AEC-Q200-006				Δ R/R: Within ±1%	
	AEC Q200 – No.22	Pressurizing force:			No visible damage		
		RLP20,32,63: 17.7N					
		RLP16: 10N					
		Test time: 6	60±1s.				

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8. Taping

- 8.1 Applicable documents JIS C 0806-3: 2014, EIAJ ET-7200C: 2010
- 8.2 Taping dimensions
- 8.2.1 Paper taping (8mm width, 4mm pitches)

Taping dimensions shall be in accordance with Figure-3 and Table-5.

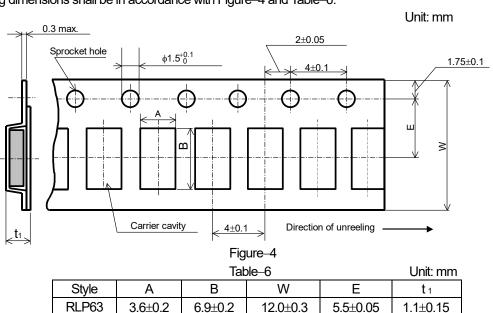


8.2.2 Embossed taping (12mm width, 4mm pitches)

Taping dimensions shall be in accordance with Figure-4 and Table-6.

2.00±0.15

RLP32



3.6±0.2

0.6±0.1

0.8max.

RLP16, 20, 32, 63 Page: 11/12

- 1). The cover tapes shall not cover the sprocket holes.
- 2). Tapes in adjacent layers shall not stick together in the packing.
- 3). Components shall not stick to the carrier tape or to the cover tape.
- 4). Pitch tolerance over any 10 pitches ±0.2mm.
- 5). The peel strength of the top cover tape shall be with in 0.1N to 0.5N on the test method as shown in the following RLP16, 20, 32: Figure–5, RLP63: Figure–6.
- 6). When the tape is bent with the minimum radius for (RLP16,20,32: 25mm, RLP63: 30mm) the tape shall not be damaged and the components shall maintain their position and orientation in the tape.
- 7). In no case shall there be two or more consecutive components missing.

 The maximum number of missing components shall be one or 0.1%, whichever is greater.

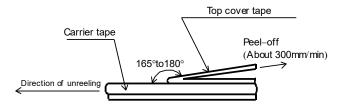


Figure-5

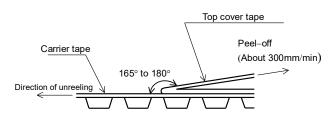
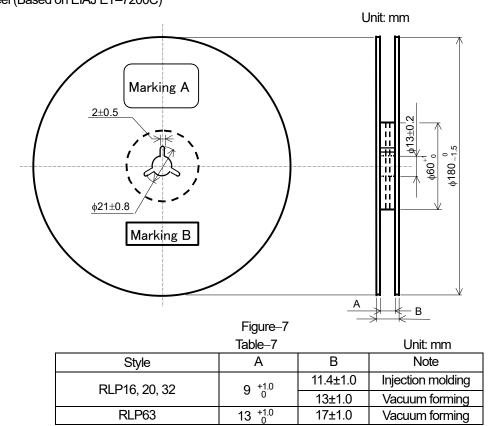


Figure-6

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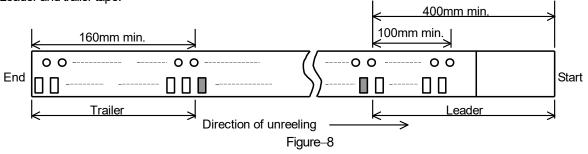
8.3 Reel dimension

Reel dimensions shall be in accordance with the following Figure–7 and Table–7. Plastic reel (Based on EIAJ ET–7200C)



Note: Marking label shall be marked on a place of Marking A or two place of Marking A and B.

8.4 Leader and trailer tape.



9. Marking on package

The label of a minimum package shall be legibly marked with follows.

9.1 Marking A

(1) Classification

(Style, Temperature coefficient of resistance, Rated resistance, Tolerance on rated resistance, Packaging form)

(2) Lot number (3) Quantity (4) Manufacturer's name or trade mark (5) Others

9.2 Marking B (KAMAYA Control label)