KAMAYA OHM

Drawing No:	RVAC-K-HTS-0002 /2
Date:	2025. 2. 7

Data sheet

Title: FIXED THICK FILM CHIP RESISTORS; RECTANGULAR TYPE AND HIGH VOLTAGE - ANTI-SULFURATION

Style: RVAC32

AEC-Q200 qualified

RoHS COMPLIANCE ITEM
Halogen and Antimony Free

Note: ・Stock conditions
Temperature: +5°C ~ +35°C
Relative humidity: 25% ~ 75%
The period of guarantee: Within 2 year from shipment by the company.
Solderability shall be satisfied.

・Product specification contained in this data sheet are subject to change at any time without notice

・If you have any questions or a Purchasing Specification for any quality agreement is necessary, please contact our sales staff.

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1. Scope

1.1 This data sheet covers the detail requirements for fixed thick film chip resistors; rectangular type and high voltage anti-sulfration, style of RVAC32

1.2 Applicable documents

JIS C 5201−1: 2011, IEC60115−1: 2008, AEC-Q200 Rev.D

2. Classification

Type designation shall be the following form.

(Example)

RVAC	32	−	475	F	TP
1	2	3	4	5	6

Style

1 Fixed thick film chip resistors; rectangular type and high voltage anti-sulfration ┐ Style

2 Size

3 Temperature coefficient of resistance

K	±100×10^{-6}/ °C
−(Dash)	Standard

4 Rated resistance

475	E24 Series, 3 digit, Ex. 475--> 4.7MΩ
1000	E96 Series, 4 digit, Ex. 1000-->100Ω 1022--> 10.2kΩ

5 Tolerance on rated resistance

D	±0.5%
F	±1%
J	±5%

6 Packaging form

TP	Paper taping

3. Rating

3.1 The ratings shall be in accordance with Table–1.

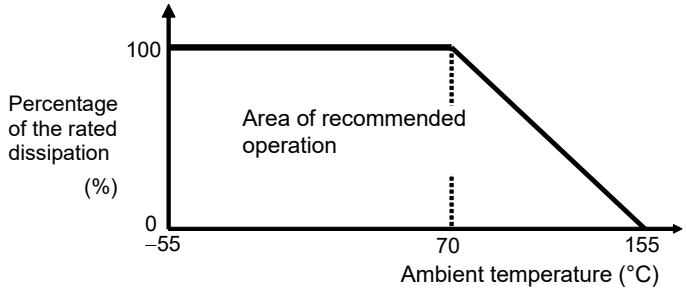
Table–1

Style	Rated dissipation (W)	Temperature coefficient of resistance (10^{-6} / °C)		Rated resistance range(Ω)	Preferred number series for resistors	Tolerance on rated resistance
RVAC32	0.25	K	±100	100~10M	E24, 96	D(±0.5%), F(±1%)
					E24	J(±5%)
		Standard	±200	47~97.6	E24, 96	D(±0.5%), F(±1%)
				47~91	E24	J(±5%)

Style	Limiting element voltage(V)	Insulation voltage (V)	Category temperature range (°C)
RVAC32	500	500	–55~+155

3.2 Derating

The derated values of dissipation at temperature in excess of 70 °C shall be as indicated by the following curve.



Figure–1 Derating curve

3.3 Rated voltage

d. c. or a. c. r. m. s. voltage calculated from the square root of the product of the rated resistance and the rated dissipation.

$$E = \sqrt{P \cdot R}$$

E : Rated voltage (V)
P : Rated dissipation (W)
R : Rated resistance (Ω)

Limiting element voltage can only be applied to resistors when the resistance value is equal to or higher than the critical resistance value.

At high value of resistance, the rated voltage may not be applicable.

4. Packaging form

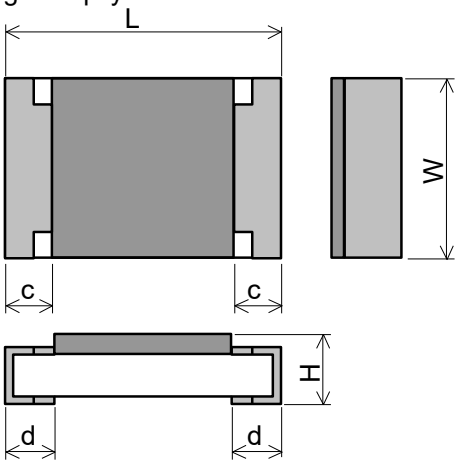
The standard packaging form shall be in accordance with Table–2.

Table–2

Symbol	Packaging form		Standard packaging quantity / units
TP	Paper taping	8mm width, 4mm pitches	5,000 pcs.

5. Dimensions

5.1 The resistor shall be of the design and physical dimensions in accordance with Figure–2 and Table–3.



Figure–2

Table–3 Unit : mm

Style	L	W	H	c	d
RVAC32	3.1 ± 0.1	1.6 ± 0.15	0.55 ± 0.10	0.5 ± 0.25	0.5 ± 0.25

5.2 Net weight (Reference)

Style	Net weight(mg)
RVAC32	9

6. Marking

The Rated resistance shall be marked in 3 digits (E24) or 4 digits (E96) and marked on over coat side.

- E24 series: 3 digits, E96 series: 4 digits

  In case of the resistance value that E96 overlaps with E24, It is marked by either.

Marking example	Contents	Application
123	12×10^{3} [Ω] → 12 [kΩ]	RVAC32
2R2	2. 2 [Ω]	Less than 10Ω of RVAC32
5623	562×10^{3} [Ω] → 562[kΩ]	RVAC32
12R7	12.7 [Ω]	RVAC32

7. Performance

7.1 The standard condition for tests shall be in accordance with Sub–clause 4.2, JIS C 5201–1: 2011.

7.2 The performance shall be satisfied in Table–4.

Table–4(1)

No.	Test items	Condition of test	Performance requirements
1	High temperature exposure AEC Q200 - No.3	MIL-STD-202 Method 108 Ambient temperature:155±2°C, Condition: Without load, Duration: 1000 $^{+48}_{0}$ h Interval measurements: 250 h and 500 h	ΔR/R: Within ±(2%+0.1Ω) No visible damage
2	Temperature cycling AEC Q200 - No.4	JESD22 Method JA-104 Temperature: -55±3°C / 125±2°C, Dwell time: 30min maximum at each temp. Transition time: 1 min. max. Number of cycles: 1000 cycles. Interval measurements: 250 cy and 500 cy	ΔR/R: Within ±(1%+0.05Ω) No visible damage
3	Bias humidity AEC Q200 – No.7	MIL-STD-202 Method 103 Condition: 85°C & 85% R.H. Test power: 10% of rated power shall be applied for continuously. Duration: 1,000 $^{+48}_{0}$ h Interval measurements: 250 h and 500 h	ΔR/R: Within ±(2%+0.1Ω) No visible damage
4	Operational life AEC Q200 – No.8	MIL-STD-202 Method 108 Ambient temperature: 125±2ºC The applied voltage shall be the voltage to be calculated at 35% of rated dissipation or the limiting element voltage whichever is the smaller. Condition: The voltage shall be applied for continuously. Duration: 1000 $^{+48}_{0}$ h Interval measurements: 250 h and 500 h	ΔR/R: Within ±(2%+0.1Ω) No visible damage
5	External Visual AEC Q200 – No.9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship.
6	Dimensions AEC Q200 – No.10	JESD22 Method JB-100	As in Table–3
7	Resistance to Solvents AEC Q200 – No.12	MIL-STD-202 Method 215 Solvent: 2−propanol at 25°C Immersion time: 3 min Brush: 10 times brushing Immersion and brush cycle: 3cycle	ΔR/R: Within ±(1%+0.05Ω) No visible damage
8	Mechanical Shock AEC Q200 – No.13	MIL-STD-202 Method 213 Waveform: half sine, Peak value100G, Normal duration 6ms Condition: XX'YY'ZZ', 10times each	ΔR/R: Within ±(0.5%+0.05Ω) No visible damage

Table–4(2)

No	Test items	Condition of test	Performance requirements
9	Vibration AEC Q200 – No.14	MIL-STD-202 Method 204 Peak acceleration and Sweep time: 5 g's for 20 min , Frequency 10Hz to 2000Hz, Condition: 12 cycles each of 3 orientations	ΔR/R: Within ±(0.5%+0.05Ω) No visible damage
10	Resistance to soldering heat AEC Q200 - No.15	MIL-STD-202 Method 210 Solder bath temp: 260±5ºC Immersed time: 10±1s	ΔR/R: Within ±(0.5%+0.05Ω) No visible damage
11	ESD test AEC Q200 – No.17	AEC-Q200-002 Human body model, 2 Kohm, 150 pF, Test voltage: 2000V	ΔR/R: Within ±(5%+0.1Ω) No visible damage
12	Solderability AEC Q200 – No.18	J-STD-002 a) Bake the sample for 155 ºC dwell time 4h / solder dipping 235ºC/ 5s. Solder: Sn96.5-Ag3-Cu0.5 b) Category 3, Solder dipping 215ºC/ 5s. Solder: Sn63Pb37 c) Category 3, Solder dipping 260ºC/ 30s.	The surface of terminal immersed shall be min. of 95% covered with a new coating of solder.
13	Electrical Characterization AEC Q200 - No.19	1. D.C. Resistance 2. Temperature Coefficient of Resistance -55 °C / +20°C +20 °C / +155°C	1. The resistance value shall correspond with the rated resistance taking into account the specified tolerance. 2. As in Table–1
14	Flammability AEC Q200 – No.20	UL-94	V-0 or V-1 are acceptable
15	Bending strength AEC Q200 – No.21	AEC-Q200-005 Bending value2mm Holding time: 60sec.	ΔR/R: Within ±(0.5%+0.05Ω) No visible damage
16	Adhesion AEC Q200 – No.22	AEC-Q200-006 Pressurizing force:17.7N Test time: 60±1s.	ΔR/R: Within ±(0.5%+0.05Ω) No visible damage
17	Flame retardance AEC Q200 – No.24	AEC-Q200-001 Test conditions: 9VDC to 32VDC Each 1h This test applies to rated voltages of 32V and above.	The following FAILURE CRITERIA does not occur. FAILURE CRITERIA - Electrically open a) A flame over 3.0 seconds duration b) An explosion c) A temperature above 350°C sustained for over 10 s

8. Taping

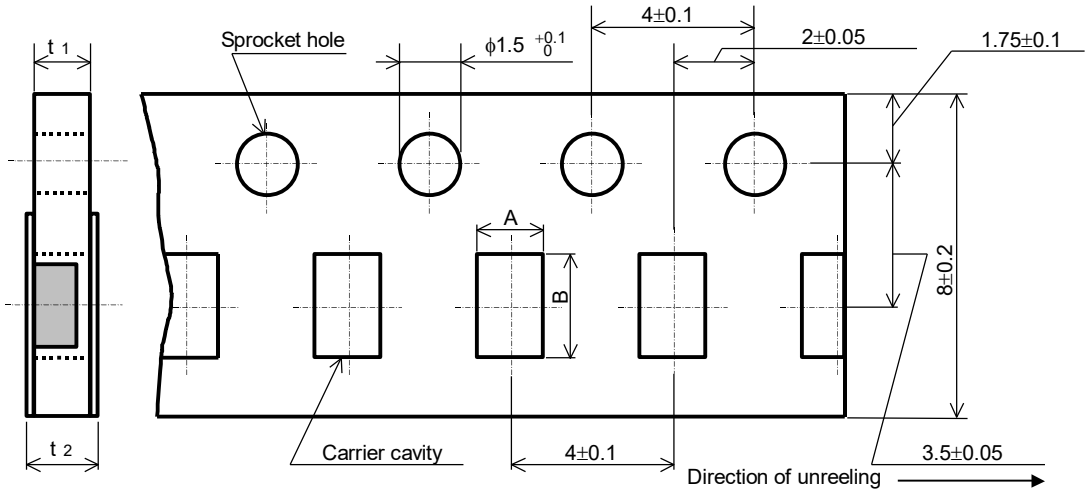
8.1 Applicable documents JIS C 0806–3: 2014, EIAJ ET–7200C: 2010

8.2 Taping dimensions

8.2.1 Paper taping (8mm width, 4mm pitches)

Taping dimensions shall be in accordance with Figure–3 and Table–5.

Unit: mm



Figure–3

Table–5 Unit: mm

Style	A	B	t_1	t_2
RVAC32	2.00±0.15	3.6±0.2	0.8±0.1	1.0max.

1). The cover tapes shall not cover the sprocket holes.

2). Tapes in adjacent layers shall not stick together in the packing.

3). Components shall not stick to the carrier tape or to the cover tape.

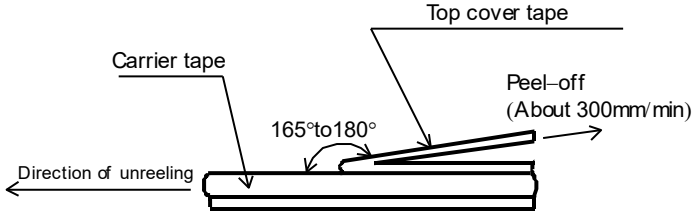
4). Pitch tolerance over any 10 pitches ±0.2mm.

5). The peel strength of the top cover tape shall be with in 0.1N to 0.5N on the test method as shown in the following Figure–4.

6). When the tape is bent with the minimum radius for 25 mm, the tape shall not be damaged and the components shall maintain their position and orientation in the tape.

7). In no case shall there be two or more consecutive components missing.
The maximum number of missing components shall be one or 0.1%, whichever is greater.

8). The resistors shall be faced to upward at the over coating side in the carrier cavity.



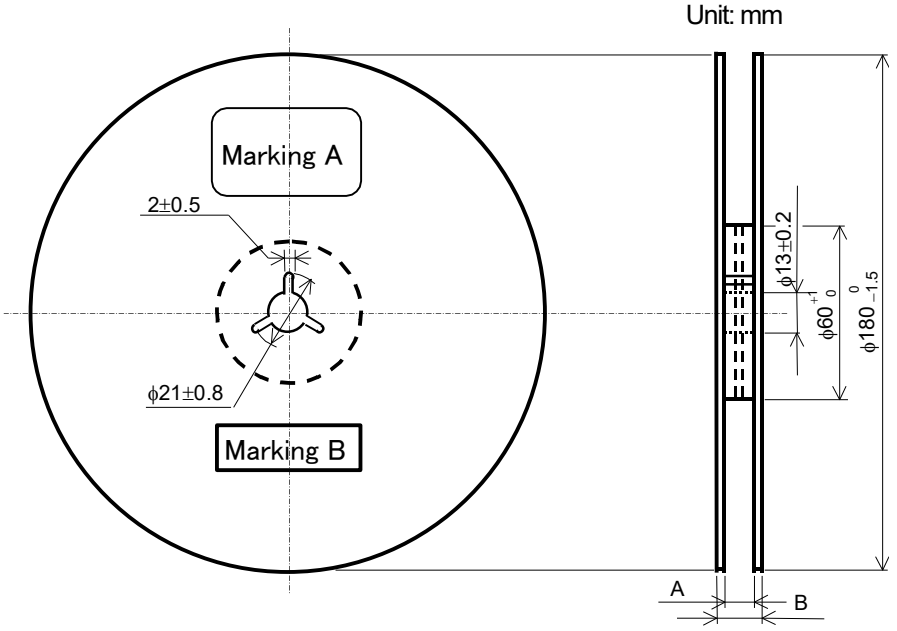
Figure–4

8.3 Reel dimension

Reel dimensions shall be in accordance with the following Figure–5 and Table–6.

Plastic reel (Based on EIAJ ET–7200C)

Unit: mm



Figure–5

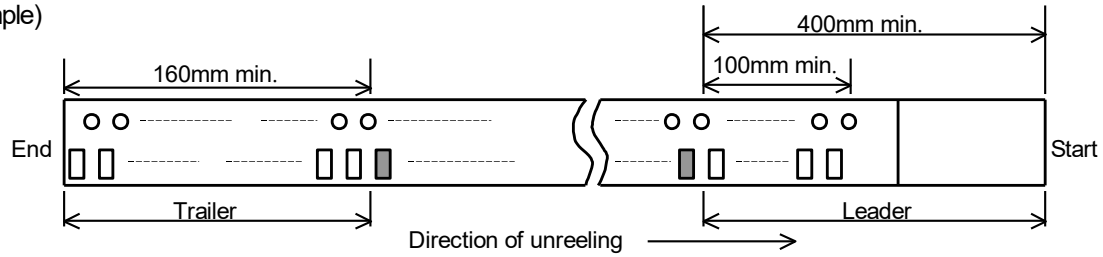
Table–6 Unit: mm

Style	A	B	Note
RVAC32	9 +1.0 0	11.4±1.0	Injection molding
		13±1.0	Vacuum forming

Note: Marking label shall be marked on a place of Marking A or two place of marking A and B.

8.4 Leader and trailer tape.

(Example)



Figure–6

9. Marking on package

The label of a minimum package shall be legibly marked with follows.

9.1 Marking A

(1) Classification

(Style, Temperature coefficient of resistance, Rated resistance, Tolerance on rated resistance, Packaging form)

(2) Quantity (3) Lot number (4) Manufacturer's name or trade mark (5) Others

9.2 Marking B (KAMAYA Control label)